

What is claimed is:

1 1. A method of manufacturing chalcogenide memory in a
2 semiconductor substrate comprising the steps of:
3 forming a N+ epitaxy layer on the semiconductor substrate;
4 forming a N- epitaxy layer on the N+ epitaxy layer;
5 forming a first shallow trench isolation (STI) in the N+
6 and N- epitaxy layers to isolate a predetermined word line
7 region;
8 forming a second STI in the N- epitaxy layer to isolate a
9 predetermined P+ doped region;
10 forming a dielectric layer on the N- epitaxy layer;
11 patterning the dielectric layer to form a first opening and
12 performing a N+ doping on the N- epitaxy layer via the first
13 opening such that a N+ doped region is formed in the N- epitaxy
14 layer and connected to the N+ epitaxy layer;
15 patterning the dielectric layer to form a second opening
16 and performing a P+ doping in the N- epitaxy layer such that
17 a P+ doped region is formed;
18 forming contact plugs in the first opening and the second
19 opening respectively; and
20 forming an electrode on each contact plug, wherein the
21 electrode includes a lower electrode, a chalcogenide layer and
22 an upper electrode.

1 2. The method as recited in claim 1, wherein the N+ epitaxy
2 layer has a thickness of 400 to 600 angstroms.

1 3. The method as recited in claim 1, wherein the N- epitaxy
2 layer has a thickness of 800 to 1200 angstroms.

1 4. The method as recited in claim 1, wherein the first STI
2 is formed in the N+ epitaxy layer and the N- epitaxy layer.

1 5. The method as recited in claim 1, wherein the first STI
2 is formed by a dry or wet etching.

1 6. The method as recited in claim 1, wherein the second STI
2 is formed by a dry or wet etching.

1 7. The method as recited in claim 1, wherein the N+ doping
2 is accomplished by implanting arsenic or phosphorus.

1 8. The method as recited in claim 7, wherein the N+ doping
2 comprises a dosage between 10^{15} and 2×10^{16} atoms/cm² and energy
3 between 10 and 30 keV.

1 9. The method as recited in claim 1, wherein the P+ doping
2 is accomplished by implanting boron.

1 10. The method as recited in claim 9, wherein the P+ doping
2 further comprising a dosage between 10^{15} and 1×10^{16} atoms/cm²
3 and energy between 1 and 3 keV.

1 11. The method as recited in claim 1, wherein the dielectric
2 layer comprises tetra-ethyl-ortho-silicate.

1 12. The method as recited in claim 1, wherein the dielectric
2 layer has a thickness of 2000 to 3000 angstroms.

1 13. A structure of chalcogenide memory, comprising:
2 a semiconductor substrate;
3 a N+ epitaxy layer formed on the semiconductor substrate;
4 a N- epitaxy layer formed on the N+ epitaxy layer;
5 a first STI formed in the N+ and N- epitaxy layers to isolate
6 a word line region;

7 a P+ doping region formed in the N- epitaxy layer;
8 a second STI formed in the N- epitaxy layer to isolate the
9 P+ doped region;
10 a N+ doped region formed in the N- epitaxy layer and
11 connected to the N+ epitaxy layer;
12 contact plugs formed on the N+ doped region and the P+ doped
13 region respectively; and
14 an electrode formed on each contact plug, wherein the
15 electrode includes a lower electrode, a chalcogenide layer and
16 an upper electrode.

1 14. The structure as recited in claim 13, wherein the N+
2 epitaxy layer has a thickness of 400 to 600 angstroms.

1 15. The structure as recited in claim 13, wherein the N-
2 epitaxy layer has a thickness of 800 to 1200 angstroms.

1 16. The structure as recited in claim 13, wherein the first
2 STI is formed in the N+ epitaxy layer and the N- epitaxy layer.

1 17. The structure as recited in claim 13, wherein the first
2 STI is formed by a dry or wet etching.

1 18. The structure as recited in claim 13, wherein the second
2 STI is formed by a dry or wet etching.

1 19. The structure as recited in claim 13, wherein the N+
2 epitaxy layer is formed by selective epitaxial method.

1 20. The structure as recited in claim 13, wherein the N-
2 epitaxy layer is formed by selective epitaxial method.